signal.

51. [Amended] The transistor of claim 50 wherein:

the semiconductor surface layer comprises p-type silicon;

the insulating layer comprises gate oxide or tunnel oxide;

the silicon carbide compound $[Si_xC_{1-x}]$ $Si_{1-x}C_x$ comprises polycrystalline silicon carbide or microcrystalline silicon carbide, or both polycrystalline and microcrystalline silicon carbide;

the source region comprises n-type silicon; and

the drain region comprises n-type silicon.

53. [Amended] The transistor of claim 50 wherein the silicon carbide compound $[Si_xC_{1-x}]$ $Si_{1-x}C_x$ is p+ doped with boron or n+ doped with phosphorus.

REMARKS

In response to the Office Action dated 6 June 2000, the applicant requests reconsideration of the above-identified application in view of the following remarks. Claims 1-15 and 22-54 are pending in the application, and are rejected. Claims 6, 7, 23, 30, 36, 49 and 54 have been cancelled. Claims 1, 11, 15, 24, 25, 27, 28, 31, 37, 38, 41, 42, 45, 46, 48, 50, 51, and 53 have been amended. No new matter has been added.

Specification

The Examiner objected to the specification. The claims have been amended to obviate the objection.

Rejections Under 35 U.S.C. § 103

Claims 1, 4-11, 14, 15, 22-26, 29-32 and 35-36 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Japanese patent document 222367 to Oyama in view of the specification. The applicant respectfully traverses.

Claim 1 recites a transistor comprising a source region, a drain region, and a channel region between the source and drain regions in a semiconductor surface layer formed on an

underlying insulating portion, and an electrically interconnected gate formed of a silicon carbide compound $Si_{1-x}C_x$, wherein x is less than 0.5, the gate being connected to receive an input signal.

Oyama is deficient in the following manner. Oyama discloses a field effect transistor (FET) with a gate electrode of silicon carbide. However, the gate of the FET of Oyama is insulated, as is clear from the title "INSULATED GATE TYPE FIELD EFFECT TRANSISTOR". The FET, shown in Figure 1(f), has a gate electrode 41 enclosed by an insulating layer 7. Therefore, Oyama does not disclose "an electrically interconnected gate formed of a silicon carbide compound $Si_{1-x}C_x$, wherein x is less than 0.5, the gate being connected to receive an input signal" as recited in claim 1.

The specification does not supply the elements that are missing in Oyama. The Examiner stated that the background of the specification teaches SOI structures. SOI technology is mentioned in the background, but the "electrically interconnected gate formed of a silicon carbide compound" recited in claim 1 is not disclosed or suggested in the background. Therefore, even as combined, Oyama and the background of the specification do not disclose or suggest all of the elements recited in claim 1. The applicant respectfully submits that claim 1 is in condition for allowance. Claims 4-10 are dependent on claim 1, and recite further limitations with respect to claim 1. For reasons analogous to those stated above, and the limitations in the claims, the applicant respectfully submits that claims 4-10 are not disclosed or suggested by the combination of Oyama and the background of the specification, and that claims 4-10 are in condition for allowance.

Claims 11, 14, 15, 22-26, 29-32 and 35-36 recite elements similar to those recited in claim 1. For reasons analogous to those stated above, and the limitations in the claims, the applicant respectfully submits that claims 11, 14, 15, 22-26, 29-32 and 35-36 are not disclosed or suggested by the combination of Oyama and the background of the specification, and that claims 11, 14, 15, 22-26, 29-32 and 35-36 are in condition for allowance.

Claims 2, 3, 12, 13, 27, 28, 33, and 34 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Oyama in view of the specification, Halvis et al. (U.S. Patent No. 5,369,040, Halvis), and Chen et al. (U.S. Patent No. 5,714,766, Chen). The applicant respectfully traverses. Neither Halvis nor Chen disclose or suggest the "electrically interconnected gate formed of a

silicon carbide compound $Si_{1-x}C_x$, wherein x is less than 0.5, the gate being connected to receive an input signal" recited in claim 1 that is missing in both Oyama and the background. Therefore, even as combined, Halvis, Chen, Oyama, and the background do not disclose or suggest all of the elements recited in claim 1.

Claims 2 and 3 are dependent on claim 1, claims 12 and 13 are dependent on claim 11, claims 27 and 28 are dependent on claim 15, and claims 33 and 34 are dependent on claim 31, and recite further limitations with respect to those claims. For the reasons analogous to those stated above, and the limitations in the claims, the applicant respectfully submits that claims 2, 3, 12, 13, 27, 28, 33, and 34 are not disclosed or suggested by the cited references, and are in condition for allowance.

Claims 37-54 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Oyama in view of Harris et al. (U.S. Patent No. 5,654,208, Harris), Lee (U.S. Patent No. 5,846,859), and Suehiro et al. (U.S. Patent No. 5,719,410, Suehiro). The applicant respectfully traverses.

None of Harris, Lee, or Suehiro disclose or suggest the "electrically interconnected gate formed of a silicon carbide compound $Si_{1-x}C_x$, wherein x is less than 0.5, the gate being connected to receive an input signal" recited in claim 1 that is missing in Oyama. Therefore, even as combined, Harris, Lee, Suehiro, and Oyama do not disclose or suggest all of the elements recited in claim 1. Claims 37-54 recite elements similar to those recited in claim 1. For reasons analogous to these, and the limitations in the claims, the applicant respectfully submits that claims 37-54 are not disclosed or suggested by the cited references, and are in condition for allowance.

CONCLUSION

The applicant respectfully submits that all of the pending claims are in condition for allowance, and such action is earnestly solicited. The Examiner is invited to telephone the below-signed attorney at 612-373-6973 to discuss any questions which may remain with respect to the present application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

LEONARD FORBES ET AL.

By their Representatives,

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Date 6 OCT 2000 By _____

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Attn: Box RCE, Washington, D.C. 20231, on this 4 day of October, 2000.

Tina Pugh
Name

Signature